

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
15 July 2004 (15.07.2004)

PCT

(10) International Publication Number  
**WO 2004/059500 A1**

(51) International Patent Classification<sup>7</sup>: **G06F 13/40**

(21) International Application Number:  
PCT/NO2002/000497

(22) International Filing Date:  
27 December 2002 (27.12.2002)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (national): AE, AG, AL, AM, AT (utility model), AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA,

CH, CN, CO, CR, CU, CZ (utility model), CZ, DE (utility model), DE, DK (utility model), DK, DM, DZ, EC, EE (utility model), EE, ES, FI (utility model), FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK (utility model), SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

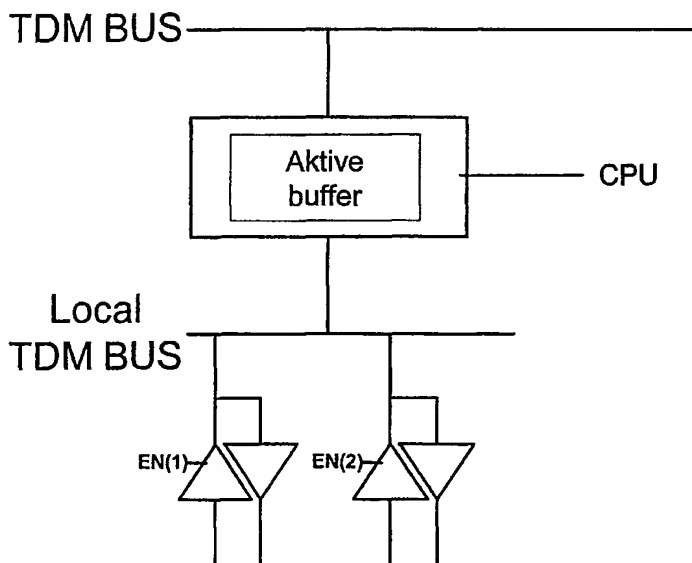
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent

[Continued on next page]

(54) Title: METHOD FOR REDUCING THE BUS LOAD IN A SYNCHRONOUS DATA BUS SYSTEM



(57) Abstract: The present invention is related to buffering between synchronous circuits communication via a global synchronous bus, and in particular an arrangement for reducing the busload in a TDM bus system by, in a preferred embodiment, introducing a local TEM data bus and an active buffer including a CPU controlled logic between the transceiver loads and the TDM bus. The active buffers in the TX and RX direction together provides a time delay for data travelling from a first local TDM bus out on the backplane TDM bus and back to a second local TDM of the exact duration of one TDM frame or an integer number of TDM frames.



(AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), *European patent*  
(AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB,  
GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR). *OAPI patent*  
(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE,  
SN, TD, TG)

— *of inventorship (Rule 4.17(iv)) for US only*

**Published:**

— *with international search report*

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